GaN MOSFET with SiO_2 Gate Oxide Deposited by Silane-Based PECVD

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For the application in the field of power electronics, enhancement mode (E-mode) is the key element for realizing safe operation and reducing power consumption due to the normally off operation. E-mode devices are also attractive for developing single-power systems and realizing low-power direct-coupled logic by the combined use of E- and D-mode devices [1]. To achieve E-mode MOSFETs on GaN, a high-quality channel with high interface carrier mobility and fewer interface states and a method to realize source and drain contact are the critical technology [2]. In this paper, we will report the performance and characteristics of a GaN MOSFET with a gate oxide deposited by silane-based plasma enhanced chemical vapor deposition and an AlGaN/GaN heterostructure as the source and drain structure.

The device structure was developed on an AlGaN/GaN HFET structure grown on a sapphire (001) substrate, including a buffer layer, a 3 μm i-GaN layer, and a 24 nm u-AlGaN layer with Al composition ratio of 25 %. To develop a GaN MOSFET structure, a two-dimensional gas (2DEG) layer is used as the ohmic contact layer, and a surface etched buffer layer is used as the channel layer, as shown in Fig. 1. The device fabrication process was started from device isolation by inductively coupled plasma (ICP) etching for an approximately 100 nm depth with $SiCl_4$ and Cl_2 gases, the AlGaN layer in the channel region was also recessed with the same ICP system using a very slow etching rate to avoid etching damage [3]. After these dry etching processes, the samples were cleaned using chemicals such as acetone and methanol, followed by wet etching with HNO_3:BHF = 1:1 solution to treat the surface. Next, a SiO_2 insulator was deposited using SAMCO PD-220LC system. Some of the fabricated samples were thermally treated under 1000 °C for 10 min in N_2 or O_2 ambient. After insulator patterning, ohmic contact was formed using Ti/Al/Ti/Au (50 nm/200 nm/40 nm/40 nm) at an annealing temperature of 850 °C for 1 min in N_2 ambient. Finally, Ni/Au (70/30 nm) was deposited as the gate metal.

Capacitance-voltage (C-V) measurement and step profile measurement by AFM showed that the thickness and permittivity of the oxide were 112.3 nm and 4.44, respectively. Enhancement-mode operation up to 15 V was confirmed. Figure 2 shows the transfer characteristics of three kinds of devices. The subthreshold swings were 91.7 and 91.1 mV/dec, respectively, for the devices treated in N_2 or O_2 ambient. Capacitance and conductance measurement showed that the field-effect mobilities were 137 and 79 cm^2/Vs, respectively, for the two devices. For comparison, subthreshold swing of 108.3 mV/dec, field-effect mobility of 108 cm^2/Vs were obtained for the device without thermal treatment. Channel mobility and interface characteristics were improved through high-temperature treatment in N_2 ambient. The mobility was degraded by treating in O_2 ambient even though the interface was improved. This is considered to be due to the oxygen diffusion into the channel.

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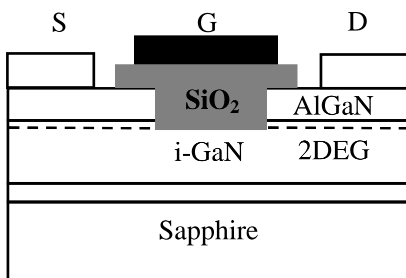

Fig. 1. Device structure of the GaN MOSFET.

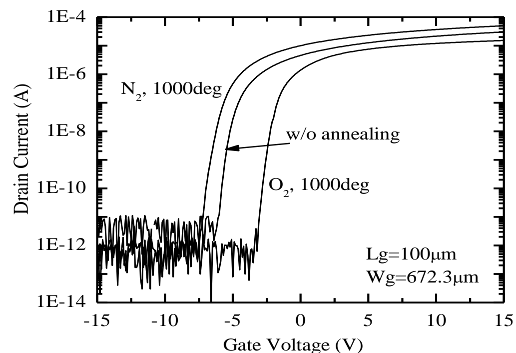

Fig. 2. Transfer characteristics of the GaN MOSFET.