Introducing GaAs Wafer Plasma Scribing with ICP Etching

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■ Introduction

Optoelectronics that utilize GaAs (Gallium Arsenide) wafers, such as LEDs, LDs and VCSELs, are widely used for various indicators, optical disks and infrared communications. The result has been the miniaturization of products, which has led to the miniaturization of corresponding devices and improved wafer efficiency.

Cutting these wafers into chips generally involves diamond scribing and dicing blades. However, such techniques create a host of problems, including 1) loss of usable wafer area because of the dicing width, and 2) physical or heat damage to the devices, making yield rates suffer as a result.

This article introduces a GaAs plasma scribing technique that uses an ICP etching system to solve these problems with narrow scribing widths, a complete lack of chipping, and scribe lines with an innovative V-shaped bottom that all result in easy breaking of GaAs.

■ Plasma Scribing Examples

GaAs wafer scribing and dicing that is a few dozen micrometers deep and utilizes resist and SiO_2 masks require high-speed, high selectivity ratio etching. Although these results can be achieved by a high-density plasma etching system, the GaAs scribing technique introduced in this article was specifically done using Samco's RIE-200iP, a high-density plasma etching system equipped with Samco's proprietary Tornado ICP coil.1)

Figure 1 illustrates the result of a chipping-free scribe line with a width of 5μm and a depth of 60μm. It was produced with an etching rate of 1.78μm/min and a resist mask selectivity ratio of 22. However, the structure of Figure 1 had an inconsistent break point due to the flat bottom of the scribe line.

Subsequently, scribe lines were etched with an innovative V-shaped bottom in order to make the break point as uniform as possible (see Figure 2).

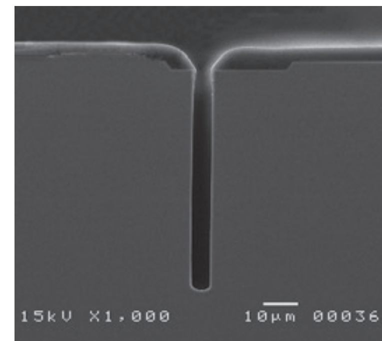

Figure 1 Example of GaAs plasma scribing with flat bottom

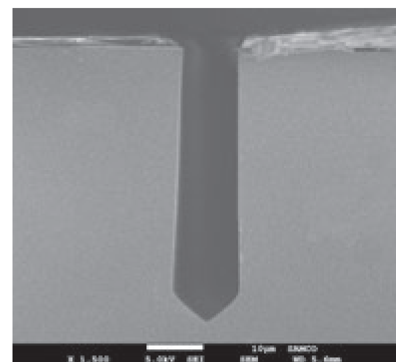

Figure 2 Example of GaAs plasma scribing with V-shaped bottom

In this case, the scribe line was etched onto a GaAs wafer with a crystal orientation of <100>. The groove width was 11μm with the resist mask, and the V-shaped bottom was anisotropically given a depth of 50μm. At the same time, the etch rate was 9.6nm/min, and

the resist mask had a selectivity ratio of 10. To confirm the etch depth's dependency on these conditions, the width of the scribing line's flat bottom portion was decreased while the etching depth was increased (see Figure 3). At a groove width of 11μm, the tapered portion connected in the same pattern as shown in Figure 2 until the scribe line reached a depth of around 50μm. Additionally, the V-shape's depth was observed to change depending on the structure's opening width.

With this scribe pattern, the breaking that follows will be much easier, and the available chip space can be maximized in a stable way.

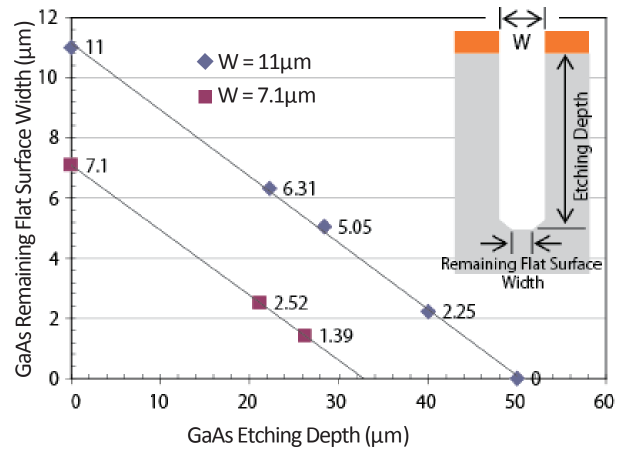

Figure 3 GaAs Plasma Scribing Etch Depth and Change in Bottom's Structure

■ Conclusion

Using Samco's RIE-200iP, it is possible to achieve anisotropic etching with high selectivity and high etching rates. This is done through plasma scribing technology capable of forming scribing lines with a V-shaped bottom.

With this method, yield rate and wafer efficiency are improved through a greater ease of breaking that results from the reduction of scribing lines and elimination of device chipping.

Although it has yet to be determined whether the same results can be achieved with compound semiconductors aside from GaAs, this technology clearly has the potential to enhance any device fabrication that requires optimal yield rates, such as the miniaturization of products.

For more information about GaAs wafer plasma scribing with ICP etching, please contact one of our representatives. We would be happy to discuss your specific process needs.

■ Reference

1) Samco Now Technical Report, vol. 79. Oct. 2012.

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