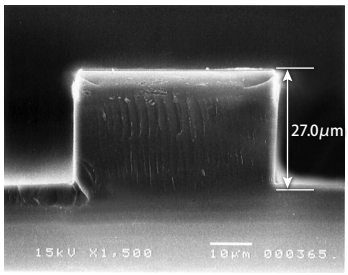
High-speed Etching of SiO_2 and SiC

The market demand for high-speed etching of SiO_2 and SiC is increasing greatly. In particular, SiC is attracting more attention as a material that enables power devices to save energy, and is highly anticipated to be the next-generation material after silicon. In the article below, SAMCO presents an introduction to the high-speed etching processes of SiO_2 and SiC.

SiO_2 Etching

SAMCO's previous record for the highest etch rate was 500nm/min on SiO_2, but recently we achieved an etch rate of 3 μm/min or more. Fig.1 shows the latest result—27.0 μm vertical etching, with an etch rate of 1.0 μm/min. The developed SiO_2 etching process can be very useful in producing optical devices, flow channels, etc.

We will further pursue better etch rates, shape control, selectivity, and uniformity, and develop the processes to provide our customers along with new R&D and production systems.



- Pattern：50μm, Line Space
- Depth：27.0μm
- Etch Rate：1.0μm/min
- Selectivity：50

Fig. 1 SiO_2 Etching Result

4H-SiC Etching

SAMCO is working on SiC etching for two processes. One is high-speed etching for VIA-hole formation, and the other is trench etching for power devices (Trench MOSFET).

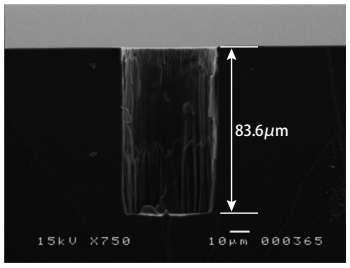
We had achieved a maximum etch rate of 1 μm/min, but experienced difficulty with shape control. However, we realized a breakthrough in this challenge, and achieved an etch rate of 3 μm/min.

The SiC etching result is shown in Fig. 2. The etch depth is 83.6 μm and the etch rate is 2.1 μm/min. Additionally, we achieved good control of the shape of the side wall, rendering it vertical.

A higher etch rate is anticipated to lead to a higher temperature of the SiC sample. The process for power device manufacturing requires a low temperature (150 ℃ or less), while it requires a high etch rate. The sample in Fig. 2 achieved high-speed etching, but exceeded 200 ℃ on the sample surface. To meet the requirements for manufacturing power devices, we fine-tuned the developed process. The result is shown in Fig. 3.

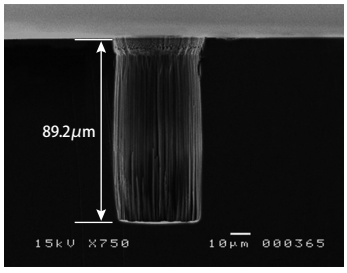
We achieved a result similar to that of the previous one. Additionally, we could maintain the sample temperature below 150 ℃. However, the SiCetch rate decreased to 1.0 μm/min, as was anticipated.

Currently, we are developing a new process that would yield high etch rates with low sample temperatures. Furthermore, we have almost completed development of the Trench MOSFET process, but are still improving the smoothness of the Trench MOS-FET gate. We will apply these new processes to develop our new R&D and production systems.



- Pattern：φ60μm Hole
- Depth：83.6μm
- Etch Rate：2.1μm/min
- Selectivity：70
- Sample Temp.：200℃+

Fig. 2 SiC Etching Result (1)



- Pattern：φ60μm Hole
- Depth：89.2μm
- Etch Rate：1.0μm/min
- Selectivity：95
- Sample Temp.：150℃ –

Fig. 3 SiC Etching Result (2)