Optimizing the SiC Plasma Etching Process For Manufacturing Power Devices

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Abstract

In this research, we optimized SiC trench etching using an ICP etching system in order to improve the problems of low SiC etching rate, low selectivity (SiC/SiO_2), and micro-trenches. The ICP etching system we used was a Samco Model RIE-600iP, which was specifically developed for the purpose of etching SiC. For this SiC trench etching study, we used SF_6, O_2, and Ar process gases. After verifying that adjusting the process parameters affected the SiC trench etching results, it became clear that we could improve the SiC etching rate by adjusting the bias power, prevent micro-trench generation by adjusting the space between the electrodes (electrode gap), and improve selectivity (SiC/SiO_2) by adjusting the process pressure. In doing so, we were able to improve the major problems of SiC trench etching. By adjusting the various parameters and optimizing the SiC trench etch, we were able to achieve an etching rate of 775 nm/min, a selectivity of 13.4 (SiC/SiO_2), and a desirable etching shape without micro-trenches.

INTRODUCTION

Power devices are used in a wide variety of fields, including consumer electronics, the automotive industry, communications, and electrical power, and these devices currently use Si as the device substrate material. However, Si-based power devices are approaching the limit of the material capabilities of Si, and it is believed that it will be very difficult to make major improvements to the current performance.

SiC has received a lot of attention in recent years as a new material for power devices. Compared to the mainstream Si, the wide-gap semiconductor SiC has excellent material qualities including high electrical breakdown strength (ten times that of Si) and thermal conductivity (three times that of Si). Current evidence suggests that SiC power devices can surpass Si power devices with high voltage endurance, low electrical resistance, high speed switching, and high temperature operation [1]. Therefore, we are actively moving forward with our research and development on power device fabrication using this material.

A broad range of technology is required for manufacturing SiC power devices. That includes the SiC plasma etching technology that is essential for manufacturing these devices. However, SiC is a difficult material to etch, as it has a high binding energy. Plasma etching of SiC often exhibits the problems of a low SiC etching rate, a low selectivity compared to the etching mask, a lack of etching control, and a rough surface after etching.

As an example of what SiC power device manufacturing demands from SiC plasma etching, we can look at SiC trench etching. SiC trench etching is required in the manufacturing of the SiC MOSFET trenches that we are actively pursuing in our research and development. In SiC trench etching, it is vital to achieve a high SiC etching rate (>500 nm/min) and high etch selectivity (SiC/SiO_2), while at the same time controlling the etching shape (perpendicular sidewalls, with no micro-trenches) and sidewall smoothness. In order to meet these challenges, it is absolutely necessary that we improve upon these problems in SiC plasma etching.

In order to improve these problem areas of SiC plasma etching, Samco Inc. developed an ICP etching system, the RIE-600iP, that was targeted for the fabrication of SiC power devices. We optimized the RIE-600iP system, and the associated SiC plasma etching process by employing our extensive experience in compound semiconductor plasma etching research. We were able to see significant improvement in the problem areas of SiC plasma etching: low SiC etching rate, low mask etch selectivity, and etching shape control.

In this paper, we will show how we optimized the SiC

plasma etching process using the RIE-600iP ICP etching system, with special attention focused on how we optimized the SiC trench etching process.

Experimental Details

The samples we used in the SiC trench etching study were 3-inch 4H-SiC wafers with a SiO_2 mask about 2 µm thick. We cleaved the wafers into chips (10 mm x 10 mm squares), and fixed them using silicon oil to a 6'' thermal-oxide-layered Si tray. The RIE-600iP ICP etching system we used in the SiC trench etching was equipped with a new uniquely optimized Tornado® ICP coil. When etching, we applied up to 2 kW of 13.56 MHz of RF power to the planar ICP coil electrode (ICP power), and up to 500W of 13.56MHz of RF power (bias power) to the lower, wafer electrode. The carrier wafer tray holding the SiC chip sample was electrostatically clamped to the bias electrode and helium backside cooled. The electrode temperature was maintained at 80°C. The clamping and helium backside cooling of the tray was key to moderating the temperature rise of the sample during the energetic etching process. We added a mechanism that allowed the lower electrode to be raised or lowered, which enabled us to change the distance (electrode gap) between the ICP coil and the lower electrode. As a means of heating the sample consistently before the start of SiC trench etching, we carried out a pre-process clean on the sample for one minute. In the pre-process, we used a mixture of O_2 and Ar. For the SiC trench etching, we used mixtures of SF_6, O_2, and Ar. In order to optimize the SiC trench etching process, we adjusted the ICP power, bias power, electrode gap, and process pressure. We used a SEM (JEOL JSM-7600F) to confirm the etching shape, etching rate, and the etch selectivity (SiC/SiO_2).

Results and Discussion

Early SiC trench etching process development exhibited problems such as SiC etching rates of less than 200 nm/min, a low etch selectivity (SiC/SiO_2) around 2-3, and micro-trench generation. Figure 1 shows a result we had from a SiC trench etching experiment in another model of the ICP etching system. The SiC trench width was 3.5 µm, the SiC etching depth was 1.9 µm, the etching rate was 186 nm/min, the selectivity (SiC/SiO_2) was 3.1, and there were undesirable micro-trenches formed along the edges of the SiC trench.

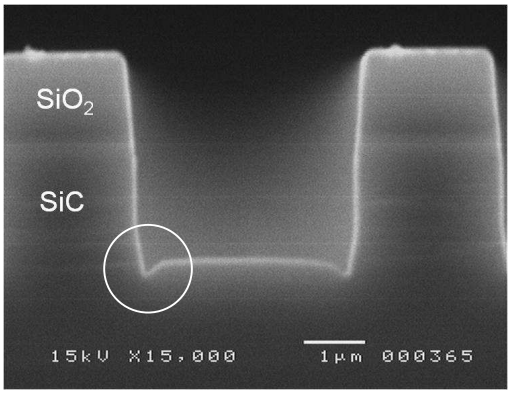


Figure 1. A 3.5 µm wide SiC trench etching result from an early SiC trench etching experiment in another ICP etching system, showing micro-trenches (white circle).

Out of the list of problems we had in our SiC trench etching development, we decided to first work on improving the low SiC etching rate. As is often seen in plasma etching of other materials, there are many cases where the etching rate goes up by increasing the ICP power and the bias power. With that in mind, we tested the possibility of increasing the SiC etching rate by increasing the ICP power and the bias power to a higher level than previous SiC trench etching processes.

It was found that the SiC etching rate did not increase significantly by increasing the ICP power. However, we did find that there was some benefit to increasing the ICP power in that with an increase in the ICP power, the etch selectivity (SiC/SiO_2) went up. For example, in the SiC trench etching process which was similar to the process used to fabricate the trench in Fig. 1, the etch selectivity (SiC/SiO_2) improved by 1.8 times by increasing the ICP power from 800W to 2kW.

The SiC etching rate was increased by increasing the bias power. Figure 2 shows the relationship between bias power and the SiC etching rate. When the bias power was increased from 100W to 500W, the SiC etching rate rose from 178 nm/min. to 412 nm/min. For the etch rate and selectivity data shown in Fig. 2, we set the ICP power to 2kW, the process pressure to 0.6 Pa, the total gas flow to 100 SCCM, and the electrode gap to 90 mm.

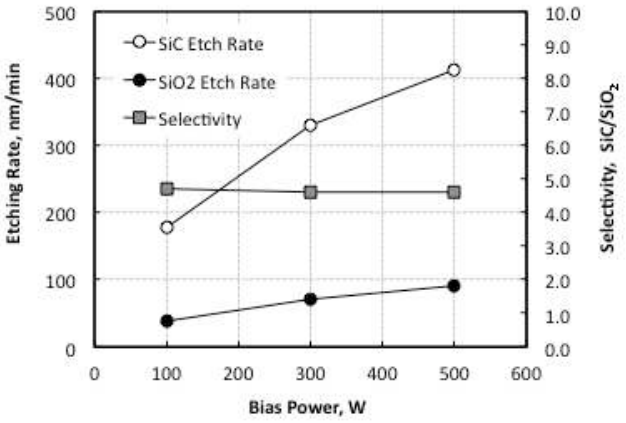
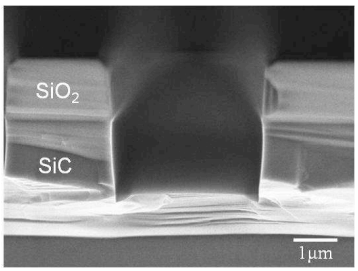


Figure 2. Relationship between bias power and SiC etching rate, SiO_2 etching rate and SiC/SiO_2 etch selectivity.

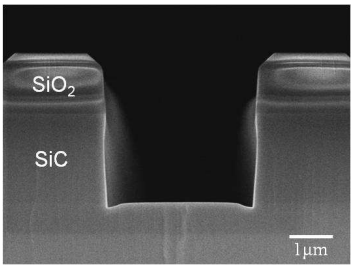
Since we had made some progress on the problems of low SiC etching rate and low selectivity, we next sought to improve the micro-trench problem. It is generally believed that micro-trenches are created by ions concentrated on the trench sidewalls. Since the amount of ion energy pulled into the sample features increases when we apply a higher bias power, we can predict that the micro-trenches would become larger with higher bias power. In contrast, when we decrease the bias power, the amount of ion energy pulled into the sample features decreases, and we can predict that the micro-trenches would become smaller. We have many etching results from ICP plasma etching of SiO_2 and other materials that proved this prediction [2]. However, despite these predictions, we learned that in SiC trench etching, increasing the bias power is effective in reducing micro-trenches.

Based on the effectiveness of increasing the bias power to reduce micro-trenches, one might also think that strengthening the self-bias (V_{dc}) would be effective as well. Although bias power tops the list for parameters that can change V_{dc}, it is possible to change V_{dc} with other parameters. At this point, we tried changing the electrode gap. V_{dc} becomes stronger by increasing the electrode gap, and weaker by decreasing it. In past SiC trench etching experiments, we set the electrode gap to 90 mm, but with the purpose of strengthening the V_{dc}, we tried setting it to 170 mm. Our results from this study found that the 170 mm electrode gap reduced the micro-trench formation more than the 90 mm electrode gap.

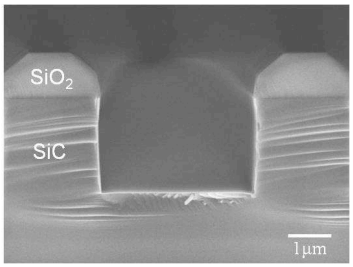
Figure 3 shows the relationship between bias power, electrode gap, and micro-trench formation. The width of the SiC trench was 3.5 µm and the etching depth was about 2 µm. For the samples shown in in Fig. 3, the ICP power was 2kW, the process pressure was 0.6 Pa, and the total gas flow was 100 SCCM. Figures 3 (a) and (b) show the relationship between bias power and micro-trench formation. When the bias power was increased from 300W to 500W, the micro-trenches became smaller. Figures 3, (b) and (c) show the relationship between the electrode gap and micro-trench formation. When the electrode gap was adjusted from 90 mm to 170 mm, the micro-trenches became smaller. For the sample shown in Fig. 3 (c), where there was no micro-trench formation, the SiC etching rate was 438 nm/min and the etch selectivity (SiC/SiO_2) was 2.8. Although we eliminated the micro-trenches by adjusting the bias power and electrode gap, the selectivity unfortunately decreased.



(a) Bias = 300W、electrode gap = 90 mm
SiC etching rate = 330 nm/min、etch selectivity（SiC/SiO_2）= 4.6



(b) Bias = 500W、electrode gap = 90 mm
SiC etching rate = 412 nm/min、etch selectivity（SiC/SiO_2）= 4.6



(c) Bias = 500W、electrode gap = 170 mm
SiC etching rate = 438 nm/min、etch selectivity（SiC/SiO_2）= 2.8

Figure 3. Relationship of bias power and electrode gap to micro-trench formation during SiC etching

After improving the low SiC etching rate and mico-trench formation problem, we focused on the task of increasing the selectivity (SiC/SiO_2) while at the same time

maintaining a high etching rate and preventing the formation of micro-trenches.

In order to raise the selectivity (SiC/SiO_2), it was necessary to either raise the SiC etching rate, and/or lower the SiO_2 etching rate. In addition to the ICP power, bias power, and the electrode gap, the process pressure was another parameter that contributed to the etching rates of the SiC and etch mask material. When we investigated the relationship between process pressure and selectivity, it became clear that raising the process pressure significantly increased the etch selectivity (SiC/SiO_2). This was because the SiC etching rate went up dramatically, while the SiO_2 etching rate dropped with increasing pressure. Figure 4 shows the relationship that process pressure has with the etching rate and etch selectivity (SiC/SiO_2). When we increased the process pressure from 1 Pa to 3 Pa, the selectivity (SiC/SiO_2) rose from 2.9 to 9.6. For the SiC etching in Figure 4, the ICP power was 2kW, the bias power was 450W, the total gas flow was 100 SCCM, and the electrode gap was 170 mm.

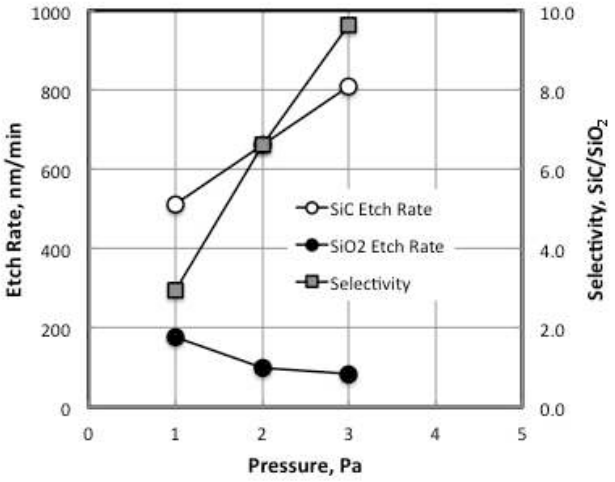


Figure 4. SiC etch rate and SiC/SiO_2 selectivity versus the process pressure

With this reported process parameter study, we were able to improve upon all of the areas in which we had problems with SiC trench etching in the past. The optimized trench etching process results are shown in Fig. 5. With a SiC trench width of 3 µm, SiC etching depth of 2.3 µm, SiC etching rate of 775 nm/min, and etch selectivity (SiC/SiO_2) of 13.4, we were also able to attain a desirable etching feature shape (perpendicular sidewall with no micro-trench). For the SiC etching in Fig. 5, the ICP power was 2kW, the bias power was 400W, the process pressure was 3 Pa, the total gas flow was 100 SCCM, and the electrode gap was 170 mm.

In order to attain the desired SiC trench etching results, it was necessary to verify the effect that adjusting each parameter had on the overall SiC etching performance, and to continue adjusting the various critical parameters until an optimized process was obtained.

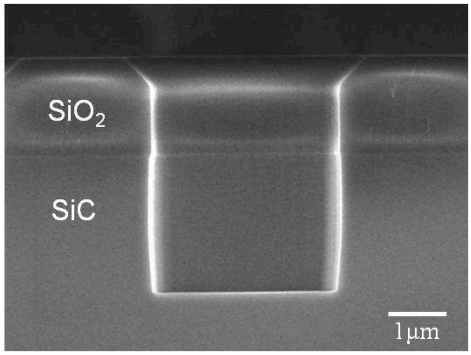


Figure 5. SiC trench etching result from optimized SiC trench etching process.

CONCLUSIONS

We optimized the SiC trench etching process parameters while utilizing a new ICP etching system. Prior to optimizing the SiC trench etching process we had problems with low etching rate, low selectivity, and micro-trench formation, but we were able to solve these problems by adjusting the ICP power, bias power, electrode gap, and process pressure. Adjusting these parameters and optimizing the SiC trench etching allowed us to achieve a high etching rate of 775 nm/min, a high etch selectivity of 13.4, and a desirable etching feature shape without the formation of micro-trenches.

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ACRONYMS

ICP: Inductively Coupled Plasma
MOSFET: Metal-Oxide Semiconductor Field-Effect Transistor
RF: Radio Frequency
SEM: Scanning Electron Microscope