Development of Backside Buried Metal Layer Technology for 3D-ICs

Naoya Watanabe[1*], Yuuki Araga[1], Haruo Shimamoto[1], Katsuya Kikuchi[1], and Makoto Nagata[2]

[1]Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology,
AIST Tsukuba Central 1, 1-1-1 Umezono, Tsukuba-shi, Ibaraki 305-8560, Japan
[2]Graduate School of Science, Technology and Innovation, Kobe University,
1-1 Rokkodai-cho, Nada-ku, Kobe 657-8501, Japan
[*]Phone: +81-29-849-1463; Fax: +81-29-862-6511
Email: naoya-watanabe@aist.go.jp

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2019/1/000268/2463217/2380-4505-2019_1_000268.pdf by guest on 22 November 2022

Abstract

In this study, we developed backside buried metal (BBM) layer technology for three-dimensional integrated circuits (3D-ICs). In this technology, a BBM layer for global power routing is introduced in the large vacant area on the backside of each chip and is parallelly connected with the frontside routing of the chip. The resistances of the power supply (V_{DD}) and ground (V_{SS}) lines consequently decrease. In addition, the BBM structure acts as a decoupling capacitor because it is buried in the Si substrate and has metal–insulator–silicon structure. Therefore, the impedance of power delivery network can be reduced by introducing the BBM layer.

The fabrication process of the BBM layer for 3D-ICs was simple and compatible with the via-last through-silicon via (TSV) process. With this process, it was possible to fabricate the BBM layer consisting of electroplated Cu (thickness: approximately 10 µm) buried in the backside of the CMOS chip (thickness: 43 µm), which was connected with the frontside routing of the chip using 9 µm-diameter TSVs.

Key words

three-dimensional integrated circuit (3D-IC), backside buried metal (BBM) layer, through silicon via (TSV), power delivery network

I. Introduction

The three-dimensional integrated circuit (3D-IC) technology with through-silicon vias (TSVs) [1]–[5] is an effective method to produce advanced, high-speed, compact, and highly functional electronic systems. However, stacking multiple chips can cause power integrity issues with respect to the circuit design. For example, IR drop in 3D-ICs increases because the number of TSVs available for power supply and ground lines is limited. Moreover, large simultaneous switching noise (di/dt noise) is generated when stacked chips are switched simultaneously in 3D-ICs. This simultaneous switching noise can generate unpredictable voltage change in the power delivery network (PDN), resulting in the system failure. To solve this power integrity issues, the impedance of the PDN must be reduced not only at the board/interposer level but also at the chip level and the reliability of power delivery must be increased. Some methods to reduce the PDN impedance at the chip level were proposed in previous studies. The first method is the widening of power/ground lines. This method is very simple but difficult to apply because wire resources are limited in the 3D ICs. The second method is the decoupling capacitor insertion technique. The metal–insulator–metal (MIM) capacitors and metal-oxide-semiconductor (MOS) capacitors are fabricated on the frontside of the tiers of 3D-ICs as on-chip decoupling capacitors [6], [7]. However, the decoupling capacitor area cannot be increased much because the decoupling capacitors are fabricated in the circuit region.

In this study, we propose the application of the backside buried metal (BBM) layer technology to each tier of 3D-ICs. Figure 1 shows the schematic illustration and equivalent circuit of BBM layer in 3D-IC. In this technology, a BBM layer is introduced in the large vacant area on the backside of each chip for global power routing, and is parallelly connected with the frontside routing of the chip. Consequently, the resistances of the power supply (V_{DD}) and ground (V_{SS}) lines decrease. In addition, the BBM structure acts as a decoupling capacitor because it is buried in the Si substrate and has MOS structure. Therefore, the impedance of the PDN can be reduced by introducing the BBM layer. The fabrication process of BBM layer for 3D-ICs is simple

and compatible with the via-last TSV process. This process primarily consists of eight steps: (1) wafer thinning, (2) deep-Si etching for TSV formation, (3) trench-Si etching for BBM formation, (4) removal of Si burr, (5) etching of bottom SiO_2 layer, (6) low-temperature chemical vapor deposition (CVD) for isolation of TSV (BBM) and Si substrate, (7) etchback and cleaning to remove the insulator from the bottom of the TSV and establish an electrical contact between the TSV and first metal layer, and (8) metal filling, chemical mechanical polishing (CMP) and wet etching. It is demonstrated that a BBM layer consisting of electroplated Cu (thickness: approximately 10 µm), which is connected with the frontside routing of the chip using 9 µm-diameter TSVs, can be fabricated.

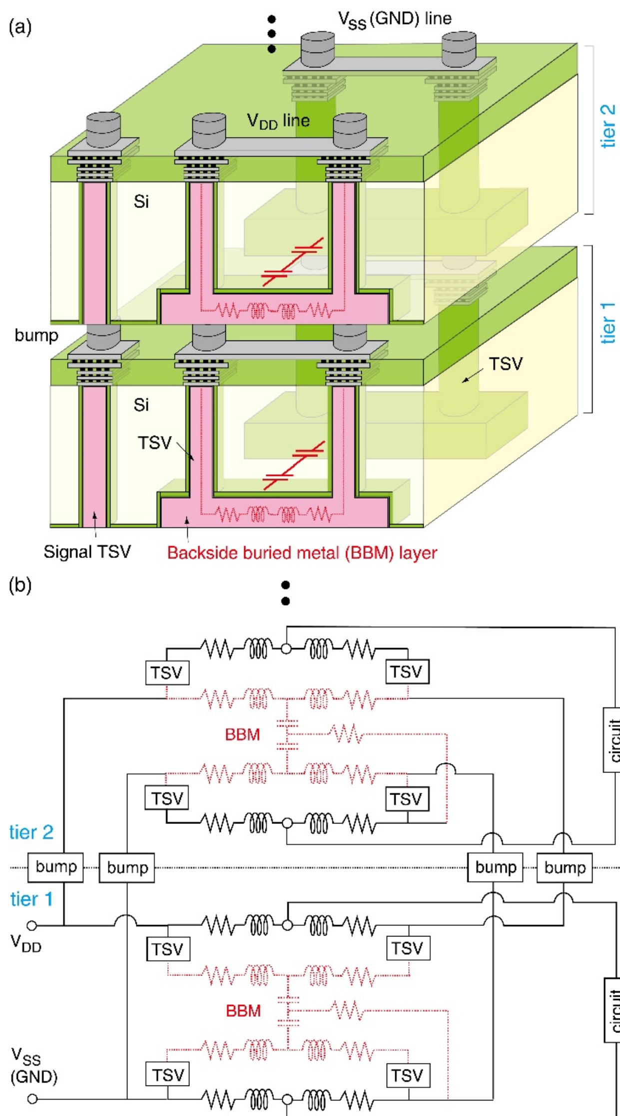

Figure 1: (a) Schematic illustration and (b) equivalent circuit of BBM layer in 3D-IC.

II. Fabrication process of BBM layer

Figure 2 shows the fabrication process of the BBM layer. The prepared wafer was an 8-inch wafer fabricated using the 0.13 µm -node CMOS technology. First, electroless Ni-Au plating and edges trimming were performed. Second, the 3M wafer support system was introduced, and the support glass was bonded with a UV-curable adhesive. The thickness of the wafer was reduced to approximately 43 µm by employing Si grinding and Si CMP using an automatic grinder/polisher (DGP8761CMP, Disco). Next, photolithography was performed using a contact aligner (MA-8, SUSS MicroTec). In this aligner, the alignment between the TSVs and the first layer of Al–Cu wiring was possible owing to the IR alignment function. The deep Si etching was performed with SF_6, Ar, and O_2 gases using a deep reactive ion etching system (Telius SP 307H, Tokyo Electron). The notching at the interface between Si and SiO_2 was suppressed by optimizing the deep Si etching time. The main etching conditions were as follows: rf power (high frequency): 500 W, rf power (low frequency): 100 W, chamber pressure: 10 Pa, and time: 7 min 5 s. After ashing, the BBM photolithography was performed. We fabricated a resist hole pattern for BBM and filled the TSV hole with a resist using the positive-tone resist and controlling the exposure time and development time. This resist protected TSV hole during the Si etching for BBM. The Si etching of BBM was also performed using SF_6, O_2, and Ar gases. The thickness of etched Si was approximately 10 µm in this study. After the removal of photoresist, we found Si burr near the hole [Fig. 3(a)]. The Si burr must be removed because it can disturb the electrical isolation between the BBM layer and Si substrate. Therefore, we removed the Si burr using SF_6 plasma etching [Fig. 3(b)]. After etching bottom SiO_2 of TSV with CF_4 gas and wet cleaning, a liner oxide was deposited with tetraethyl orthosilicate and O_2 gases using a CVD system (PD-330STC, Samco) at the deposition temperature of 150 °C. Then, etchback was performed to remove the oxide from the bottom of the TSVs and expose the first metal layer (Al–Cu wiring). The exposed first metal layer was wet cleaned using an organic alkaline solution (PK-DEX4000F, PARKER CORPORATION) to remove contaminants (reaction products generated by etchback) (Fig. 4) [8]. This cleaning is crucial for the fabrication of high-yield TSV/BBM. After Ar ion cleaning, a Ti-Cu film was deposited using ionized sputtering, and Cu electroplating was carried out for Cu filling. Then, copper CMP and Ti etching were performed. After bonding the dicing tape, the support glass was debonded by laser irradiating the light-to-heat conversion (LTHC) layer of the support glass, and the adhesive was debonded by manual peeling. Finally, the thin wafer was diced, and the diced chips were selected and placed on a tray.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2019/1/000268/2463217/2380-4505-2019_1_000268.pdf by guest on 22 November 2022

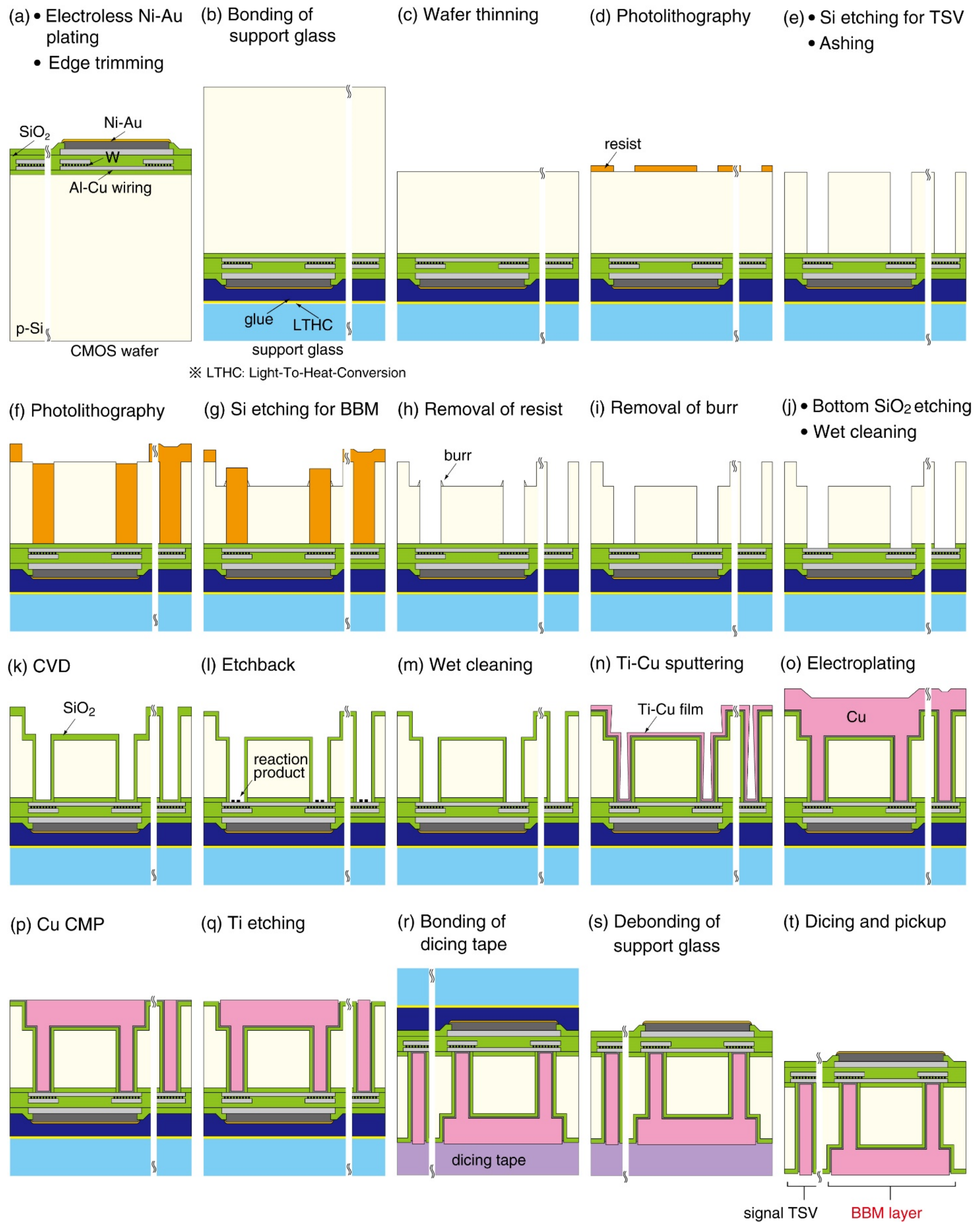

Figure 2: Fabrication process of BBM layer, which is fully compatible with the via-last TSV process.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2019/1/000268/2463217/2380-4505-2019_1_000268.pdf by guest on 22 November 2022

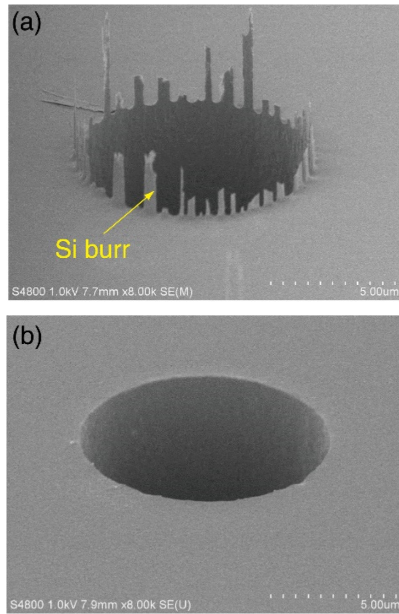

Figure 3: Scanning electron microscope (SEM) images of Si region near hole. (a) after photoresist removal. (b) after SF_6 plasma etching. The Si burr was removed using SF_6 plasma etching.

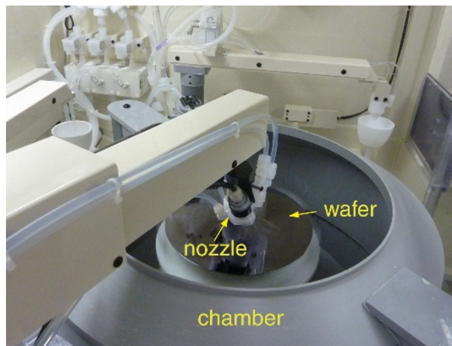

Figure 4: Wet cleaning of the first metal layer.

Figure 5 shows the cross-sectional SEM images of signal TSVs. The diameter and depth of signal TSV were approximately 10 µm and 40 µm, respectively. The notching between Si and SiO_2 was small (below 0.5 µm) owing to the optimization of the deep Si etching condition. On the other hand, the Ti etched region was generated because of the removal of Ti layer due to wet etching. This Ti etched region can be reduced by applying the CMP process for the removal of Ti layer.

Figure 6 shows the cross-sectional SEM images of the BBM layer. The BBM layer (thickness: approximately 10 µm) was connected with the first metal layer (Al-Cu wring) using 9 µm-diameter TSVs. In addition, this BBM layer could be fabricated simultaneously with the signal TSVs.

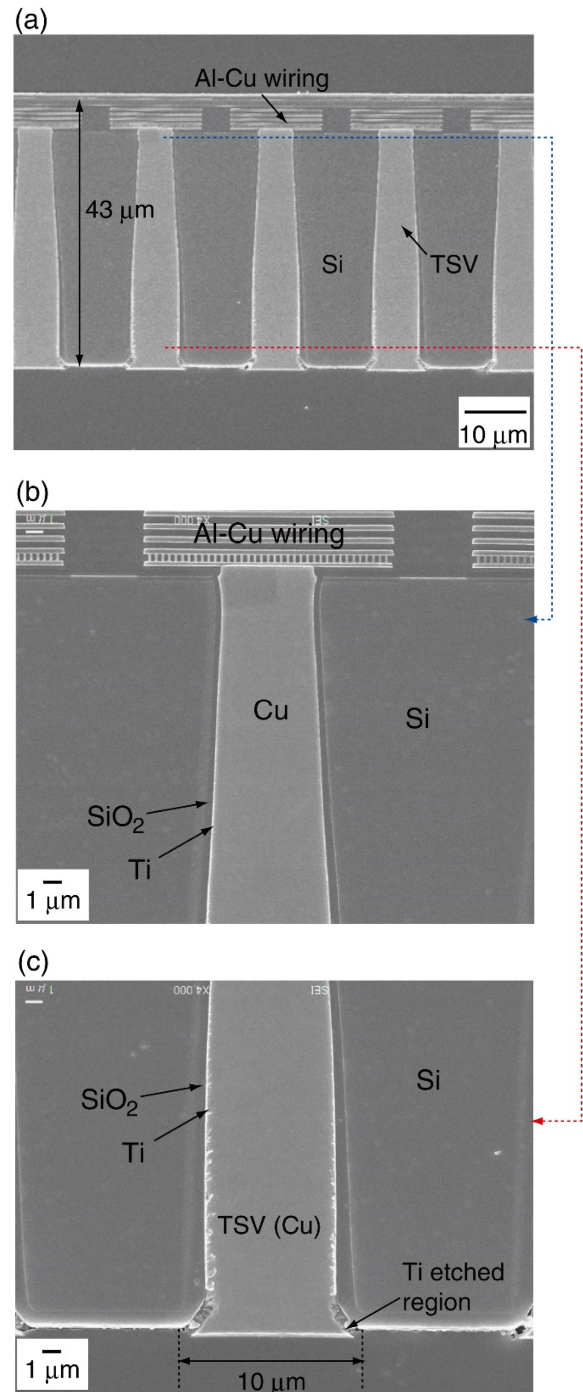

Figure 5: Cross-sectional SEM images of signal TSVs. The diameter and depth of signal TSV were approximately 10 µm and 40 µm, respectively. The notching was small (below 0.5 µm). On the other hand, the Ti etched region was generated due to the wet etching of Ti layer.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2019/1/000268/2463217/2380-4505-2019_1_000268.pdf by guest on 22 November 2022

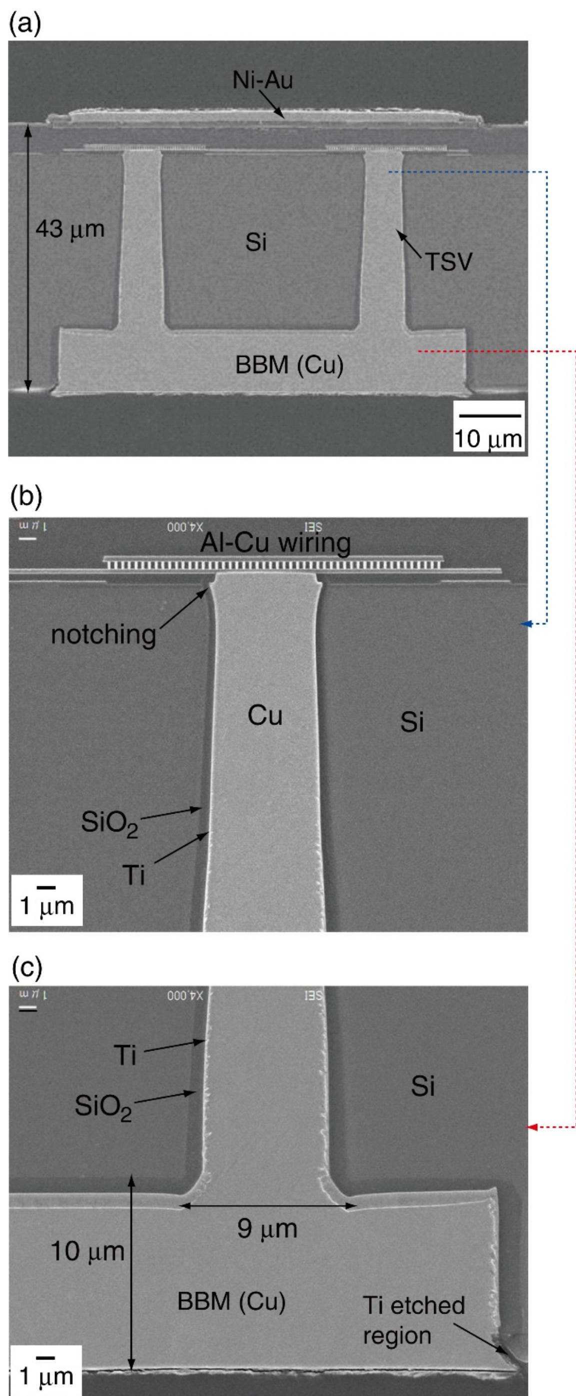

Figure 6: Cross-sectional SEM images of BBM layer. The BBM layer was connected with the first metal layer (Al-Cu wiring) using TSVs. The thickness of BBM layer was approximately 10 μm. The notching was small (below 0.5 μm). On the other hand, the Ti etched region was generated due to the wet etching of Ti layer.

III. Electrical characteristics of BBM layer

In order to confirm the effectiveness of BBM layer, we investigated the fundamental electrical characteristics of BBM layer.

Table I shows the fundamental electrical characteristics of the BBM layer, which were obtained using a precision semiconductor parameter analyzer (4156C, Keysight) and an LCR meter (4284A, Keysight). The resistance of 15 μm-width BBM layer and TSV (connected with BBM) was low. The capacitance between 15 μm-width 2.5 mm-length BBM layer and Si substrate was not relatively large. However, by using 'free space' (backside of CMOS chip) and arranging multiple BBM patterns in parallel, a large capacitance can be obtained, and the BBM layer will act as a decoupling capacitor.

Table I: Fundamental electrical characteristics of BBM layer.

	Value
Resistance of TSV conncted with BBM layer	25 mΩ
Resistance of 15 μm-width BBM layer	0.16 mΩ/μm
Capacitance between Si substrate and 15 μm-width 2.5 mm-length BBM layer	6.0 pF

※ Thickness of BBM layer: 10 μm

IV. Conclusion

In order to solve the power integrity issues of 3D-ICs, we developed a simple process to fabricate a BBM layer in CMOS chip, which was fully compatible with a via-last TSV process. Although this process appears to be similar to the dual-damascene process [9], there are a few differences because the BBM in the proposed process is fabricated not in the insulating film but in the Si substrate. With this process, it was possible to fabricate the BBM layer consisting of an electroplated Cu (thickness: approximately 10 μm) buried in the backside of the CMOS chip (thickness: 43 μm), which was connected with the frontside routing of the chip using 9 μm-diameter TSVs. In addition, this BBM layer could be fabricated simultaneously with the signal TSVs.

This BBM layer technology will improve the power integrity of 3D-ICs and contribute to their overall performance enhancement.

Acknowledgment

This paper is based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO). The authors would like to express gratitude to Mr. S. Ukita and

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2019/1/000268/2463217/2380-4505-2019_1_000268.pdf by guest on 22 November 2022

Mr. H. Suzuki of the National Institute of Advanced Industrial Science and Technology for their technical assistances.

References

[1] M. Koyanagi, Y. Nakagawa, K. W. Lee, T. Nakamura, Y. Yamada, K. Inamura, K. T. Park, and H. Kurino, "Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology," ISSCC Dig. Tech. Papers, 2001, p. 270.

[2] N. Watanabe, I. Tsunoda, T. Takao, K. Tanaka, and T. Asano, "Fabrication of Back-Side Illuminated Complementary Metal Oxide Semiconductor Image Sensor Using Compliant Bump," Jpn. J. Appl. Phys., vol.49 (2010) 04DB01.

[3] D. H. Kim, K. Athikulwongse, M. Healy, M. Hossain, M. Jung, I. Khorosh, G. Kumar, Y. J. Lee, D. Lewis, T. W. Lin, C. Liu, S. Panth, M. Pathak, M. Ren, G. Shen, T. Song, D. H. Woo, X. Zhao, J. Kim, H. Choi, G. Loh, H. H. Lee, and S. K. Lim, "3D-MAPS: 3D Massively Parallel Processor with Stacked Memory," ISSCC Dig. Tech. Papers, 2012, p.188.

[4] C. Erdmann, D. Lowney, A. Lynam, A. Keady, J. McGrath, E. Cullen, D. Breathnach, D. Keane, P. Lynch, M. D. L. Torre, R. D. L. Torre, P. Lim, A. Collins, B. Farley, and L. Madden, "A Heterogeneous 3D-IC Consisting of Two 28 nm FPGA Die and 32 Reconfigurable High-Performance Data Converters," IEEE Journal of Solid-State Circuits, vol. 50 (2015) 258.

[5] T. Haruta, T. Nakajima, J. Hashizume,T. Umebayashi, H. Takahashi, K. Taniguchi, M. Kuroda, H. Sumihiro1, K. Enoki, T. Yamasaki, K. Ikezawa, A. Kitahara, M. Zen, M. Oyama, H. Koga, H. Tsugawa, T. Ogita, T. Nagano, S. Takano, and T. Nomoto, "A 1/2.3inch 20Mpixel 3-Layer Stacked CMOS Image Sensor with DRAM," ISSCC Dig. Tech. Papers, 2017, p. 76.

[6] P. Zhou, K. Sridharan, and S. S. Sapatnekar, "Congestion-aware Power Grid Optimization for 3D Circuits Using MIM and CMOS Decoupling Capacitors," Proceedings of Asia and South Pacific Design Automation Conference, 2009, p. 179.

[7] P. Zhou, K. Sridharan, and S. S. Sapatnekar, "Optimizing Decoupling Capacitors in 3D Circuits for Power Grid Integrity," IEEE Design & Test of Computers, vol. 26 (2009) 15.

[8] N. Watanabe, H. Kikuchi, A. Yanagisawa, H. Shimamoto, K. Kikuchi, M. Aoyagi, and A. Nakamura, "Development of a High-Yield Via-Last Through Silicon Via Process Using Notchless Silicon Etching and Wet Cleaning of the First Metal Layer," Jpn. J. Appl. Phys., vol. 56 (2017) 07KE02.

[9] C. W. Kaanta, S. G. Bombardier, W. J. Cote, W.R. Hill, G. Kerszykowski, H. S. Landis, D.J. Poindexter, C. W. Pollard, G.H. Ross, J.G. Ryan, S. Wolff, and J. E. Cronin, "Dual Damascene: a ULSI wiring technology," Proceedings of Eighth International IEEE VLSI Multilevel Interconnection Conference, 1991, p. 144.

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2019/1/000268/2463217/2380-4505-2019_1_000268.pdf by guest on 22 November 2022