

# Recess Etching Process for AlGa<sub>N</sub>/Ga<sub>N</sub>-HFET Devices Using In-Situ Monitoring

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## Abstract

SAMCO has developed a dry etching process for AlGa<sub>N</sub>/Ga<sub>N</sub>-HFET power devices with precise control of the etching film depth. AlGa<sub>N</sub>/Ga<sub>N</sub>-HFET devices are “normally on” and require a circuit to turn off the device. To avoid the turning-off of devices, “normally off” devices are preferred for power device applications. One method of making AlGa<sub>N</sub>/Ga<sub>N</sub>-HFET devices “normally off” is to eliminate the 2D electron gas channel under the gate electrode. This can be achieved by recess etching (for example, etching a 25 nm AlGa<sub>N</sub> layer with less than 5 nm of the AlGa<sub>N</sub> film remaining). Precise control of the remaining AlGa<sub>N</sub> layer thickness is the most crucial factor because the remaining AlGa<sub>N</sub> layer depth determines  $V_g$ - $I_d$  characteristics of AlGa<sub>N</sub>/Ga<sub>N</sub>-HEFT devices (when  $V_d$  is constant).

Remaining AlGa<sub>N</sub> layer thickness was controlled by the etching time while carrying out very slow etching. However, the recess etching requires thickness control on the order of 1 nm and this timed etching method does not allow that. Since the AlGa<sub>N</sub> etch rate can change due to byproducts in the reaction chamber, the timed etching approach is clearly not effective. This paper introduces SAMCO's development of a new, precise method for control of the remaining AlGa<sub>N</sub> layer thickness during recess etching. SAMCO's new method employs an interferometric film thickness measurement system and in-situ monitoring of the remaining AlGa<sub>N</sub> thickness.

## INTRODUCTION

Next generation power devices using Gallium Nitride (Ga<sub>N</sub>) and Silicon Carbide (SiC) have excellent power consumption and miniaturization characteristics, and research efforts have been aimed at introducing the devices into market. The key processes for realizing power devices are: (1) for Ga<sub>N</sub> power devices, gate etching to convert the AlGa<sub>N</sub>/Ga<sub>N</sub>-HFET devices into normally-off operation, and passivation layer formation to suppress current collapse, and (2) for SiC power devices, trench formation etching, via hole formation etching, and gate insulation film formation. SAMCO has developed PECVD and ICP-RIE systems to achieve the requirements of the key processes mentioned

above. In this report, highly precise recess etching technology for Ga<sub>N</sub> power devices is described.

Table I, summarizes the important semiconductor material characteristics [1] of Si, GaAs, Ga<sub>N</sub> and 4H-SiC (for which power device commercialization has already started),  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> (which has recently come into the spotlight), and diamond (which is still in the research stage but shows promise). The most important characteristics for power device applications are wide band-gap, high breakdown voltage, and high thermal conductivity. Also, high electron mobility, high hole mobility, high saturation velocity, and low dielectric constant are important for high speed response characteristics. Diamond shows extraordinary performance but has fundamental disadvantages, such as the difficulties of growing large single crystal substrates and in P-N doping control.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has a wide band gap, high breakdown voltage, and n-type control is possible by doping with Sn. Hetero-junctions with other oxide semiconductors and MOS-FET fabrication is also possible using  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. However, it has the disadvantage of having an extremely low thermal conductivity.

4H-SiC is a power device material whose power device commercialization has already started. High quality epitaxial growth is possible because 4H-SiC substrates are available in the market, and Schottky Barrier Diodes (SBDs) and Double-diffused Metal-Oxide-Semiconductor Field Effect Transistors (DMOS-FETs) have been already commercialized. Furthermore, there have been research and development activities on MOS-FETs with vertical device structure, Insulated Gate Bipolar Transistor (IGBT), and Junction FET (SIT = Static Induction Transistor). Ga<sub>N</sub> is anticipated to show better performance than 4H-SiC. Ga<sub>N</sub> substrates are grown using a Na flux method but are not easy to obtain. Therefore epitaxial growth is achieved using buffer layers on sapphire or Si substrates to mitigate the difference in lattice constants. Ga<sub>N</sub> on sapphire has been applied to AlGa<sub>N</sub>/Ga<sub>N</sub>-HFET (Hetero-structure FET) and Ga<sub>N</sub>-MOSFET devices with planar structure. Both power device and high-speed device applications are possible.

TABLE I.  
SEMICONDUCTOR MATERIAL PROPERTIES

Material		Si	GaAs	Diamond	GaN	4H-SiC	$\beta$ -Ga <sub>2</sub> O <sub>3</sub>
Band-gap	E <sub>g</sub> (eV)	1.1	1.4	5.45	3.39	3.26	4.8
Electron Mobility	$\mu_e$ (cm <sup>2</sup> /V•s)	1,400	8,500	2,200	900	1,000/850	~ 300
Hole Mobility	$\mu_h$ (cm <sup>2</sup> /V•s)	600	400	1,600	150	115	
Breakdown Voltage	E <sub>c</sub> (MV/cm)	0.3	0.4	10	3.3	2.5	8
Saturation Velocity	V <sub>sat</sub> (10 <sup>7</sup> cm/s)	1	2	2.7	2.7	2.2	
Intrinsic Carrier Concentration	n <sub>i</sub> (cm <sup>-3</sup> )	1.5x10 <sup>10</sup>	1.8x10 <sup>6</sup>	1.6x10 <sup>-27</sup>	1.9x10 <sup>-10</sup>	8.2x10 <sup>-9</sup>	
Thermal Conductivity	$\lambda$ (W/cm/K)	1.5	0.5	20	2	4.9	0.14
Relative Dielectric Constant	$\epsilon$	11.8	12.8	5.5	9	9.7	10
Bulk Material (substrate)		Com	Com	Res	Res	Com	Com
Com = Commercial, Res = Research							
Band Structure (Direct/Indirect)		I	D	I	D	I	D

GaN-based devices are also promising substitutes for AlGaAs/GaAs-HFET devices.

AlGa<sub>N</sub>/GaN-HFET devices are fabricated with undoped GaN and undoped AlGa<sub>N</sub> epitaxially grown on Si or sapphire substrates. Source, Drain, and Gate electrodes are formed on the layers. The ratio of Al in the AlGa<sub>N</sub> layer is ~0.25 and AlGa<sub>N</sub> thickness is approximately 25 nm. Through the Piezo effect, highly concentrated 2DEG (2 Dimensional Electron Gas) is formed at the AlGa<sub>N</sub>/GaN interface, resulting in the device becoming “Normally ON”. However “Normally OFF” is more preferable for power devices. In order to form “Normally OFF” devices and to decrease the ON resistivity, three methods are used: (1) make the device a MOS-FET, (2) use a p-GaN GIT (Gate Injection Transistor), or (3) use a recess structure by thinning the AlGa<sub>N</sub> layer to less than 5 nm. These methods will all eliminate 2DEG at the gate electrode. Gate formation is the most important technology in the fabrication process of AlGa<sub>N</sub>/GaN-HFET devices from the viewpoint of Gate voltage (V<sub>g</sub>) – Drain current (I<sub>d</sub>) characteristics (Drain voltage (V<sub>d</sub>) = constant).

#### EXPERIMENTAL DETAILS

In this research, etching of AlGa<sub>N</sub> and GaN, and deposition of SiO<sub>2</sub> were carried out on SAMCO RIE-200iPC and PD-220LC systems, respectively. These systems are displayed in Images 1 and 2 below.

Research on “Normally Off” devices was carried out with three types of gate structures as follows;

- 1) MOS-FET
- 2) GIT (Gate Injection Transistor)
- 3) Recess etching

For the MOS-FET gate structure, AlGa<sub>N</sub> was etched to the GaN layer, the SiO<sub>2</sub> gate oxide was deposited, and the device characteristics were studied. For the GIT, high selectivity etching of GaN/AlGa<sub>N</sub> was carried out. For the recess etching, highly precise etching of AlGa<sub>N</sub> was carried

out to control its thickness using in-situ monitoring.



Image 1 – RIE-200iPC



Image 2 – PD-220LC

#### RESULTS AND DISCUSSION

1) *AlGa<sub>N</sub>/GaN MOS-FET*. Figure 1 illustrates the MOS-FET structure. The AlGa<sub>N</sub> layer at the gate was etched down to the GaN interface using an ICP-RIE process. In order to obtain smooth surfaces that would suppress plasma damage, slow etching was carried out at the rate of about 1 nm/min. Surface smoothness (RMS) was essentially constant before (0.4 nm) and after (0.41 nm) the etching [2]. A 100 nm thick gate oxide was formed using a plasma enhanced CVD process and a SiH<sub>4</sub>-N<sub>2</sub>O process gas mixture. Following deposition of the gate oxide it was annealed in a N<sub>2</sub> environment at 1000°C. Highly concentrated 2DEG is generated at the AlGa<sub>N</sub>/GaN interface. Since the Source and Drain are formed on the AlGa<sub>N</sub> layer. As a result, Drain voltage-current characteristics showed saturation, and control with Gate voltage was possible. Additionally, channel mobility was approx. 150 cm<sup>2</sup>/V • s, and an excellent interface condition between Gate oxide and GaN of 10<sup>11</sup>/cm<sup>2</sup>-eV was obtained [3]. Mobility was about 10% HFET mobility. From these

results, it can be concluded that plasma damage was suppressed.

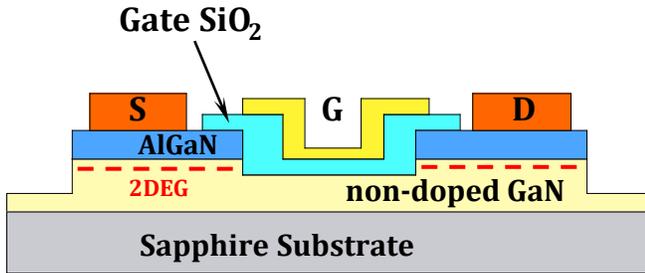


Figure 1. MOS-FET structure

2) *GIT AlGaN/GaN-HFET*. Fig. 2 illustrates the GIT AlGaN/GaN-HFET structure [4], [5]. The GaN layer, AlGaN layer, and p-GaN layers were epitaxially grown on Si or sapphire substrates. By growing p-GaN at the Gate, a depletion layer is formed and 2DEG can be eliminated. Etching with high AlGaN/GaN selectivity so that the ICP-RIE etch rate decreases significantly at the AlGaN layer is required to achieve this structure. Fig. 3 illustrates the selectivity of GaN/AlGaN (Blue) and GaN etching rate (Green) when the sample was etched using Cl<sub>2</sub>/Ar/O<sub>2</sub> with O<sub>2</sub> flow as a parameter. With 2 SCCM of O<sub>2</sub> flow, a GaN etch rate of 70 nm/min and GaN/AlGaN selectivity of 55 was achieved. Through further process development, an optimal GaN/AlGaN selectivity of 100 was obtained (red symbol). Additionally, highly selective etching is required to obtain excellent uniformity over the wafer.

3) *Recessed Gate AlGaN/GaN-HFET*. In Fig. 4, an AlGaN/GaN-HFET device with recess gate structure is shown. Here the device with a “Normally OFF” characteristic is the target, and suppressing plasma damage as well as controlling the residual AlGaN thickness to under 5 nm at the Gate is required to achieve low ON-resistance (decrease resistivity between Source – Gate and Drain – Gate). Furthermore, uniform etching across the wafer is required so that the device characteristic distribution such as the Gate voltage/Drain current (with constant Drain voltage) stays within the acceptable range.

As shown in Fig. 5, Super slow etching of 0.8nm/min (0.013nm/sec) was achieved by decreasing Bias RF power. With super slow etching, batch to batch distribution of etch depth by time control was minimized and the precision of etch depth control was improved. Furthermore, an excellent profile without micro trenches, pits, or pillars was achieved, as shown in Fig. 6. Cross wafer uniformity was ±2.5% for 6 inch wafers.

At the time of recess etching, an interferometry type End Point Detector (EPD) was used to monitor the etch depth.

The results of interferometry monitoring are shown in Fig. 7 (time vs. reflection intensity of 364 nm light).

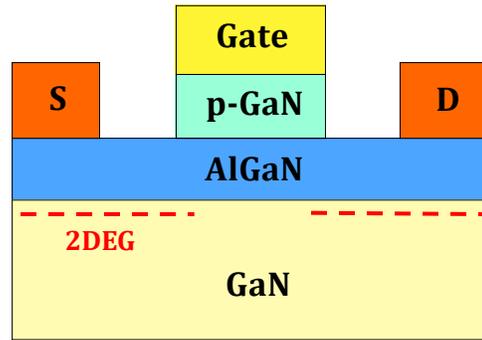


Figure 2. Gate Injection Transistor (GIT) AlGaN/GaN-HFET structure

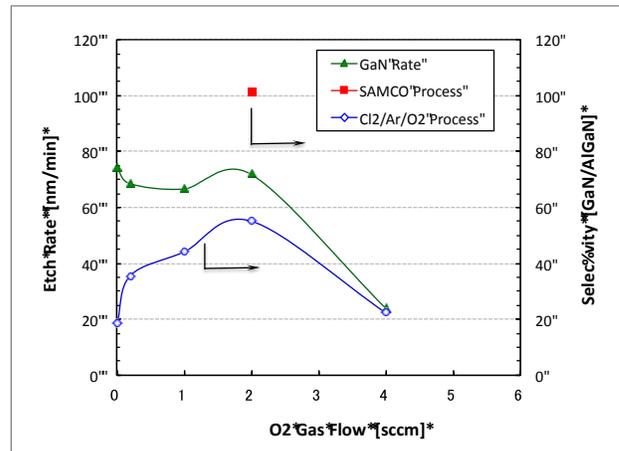


Figure 3. GaN/AlGaN highly selective etching

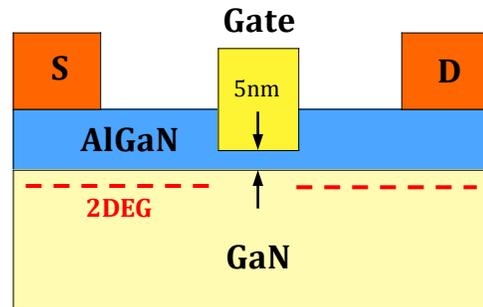


Figure 4. Recess gate structure for AlGaN/GaN-HFET

It is well known that interface information can be detected using the refractive index difference of GaN and AlGaN layers. Furthermore, by optimizing a relevant formula, Fig. 8 was obtained to show the etch time to reach the GaN layer and residual layer thickness (with initial AlGaN layer thickness of 25 nm). On the other hand, the etched sample was observed using AFM and it was found that the etch depth was 20 nm, and this coincided well with the result of Fig. 8.

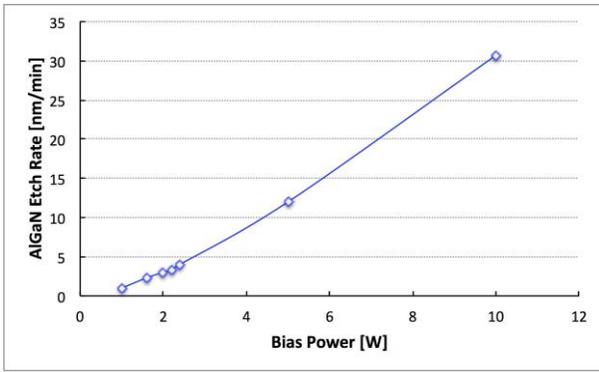


Figure 5. RF bias power and AlGaN etching rate

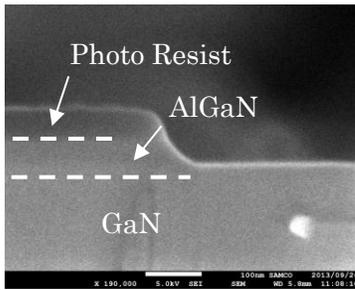


Figure 6. Cross sectional SEM of gate recess using super slow etching

As shown above, SAMCO's recess etching process with the combination of super slow etching and interferometry type EPD enables highly precise etching with a precision range of  $\pm 1\text{nm}$ . Furthermore, this method can be applied to the highly selective etching at the interface of GIT AlGaN/GaN-HFET (etching p-GaN layer and stopping at AlGaN layer) as described in subsection 2) above.

#### CONCLUSIONS

SAMCO has successfully developed ICP-RIE etching technology with low plasma damage, and surface smoothness to achieve "Normally OFF" GaN-based power devices. Etch-stop technology to precisely control the etch depth of AlGaN using an interferometry EPD, in particular, is crucial to achieving the recess structure. This technology can be applied to other processes involving the etching of layers with different refractive indices. Additionally, though not described in this report, SAMCO has been developing PECVD technology to suppress current collapse. System and process development are now under way for other power device materials such as 4H-SiC, taking the 4H-SiC market potential into consideration.

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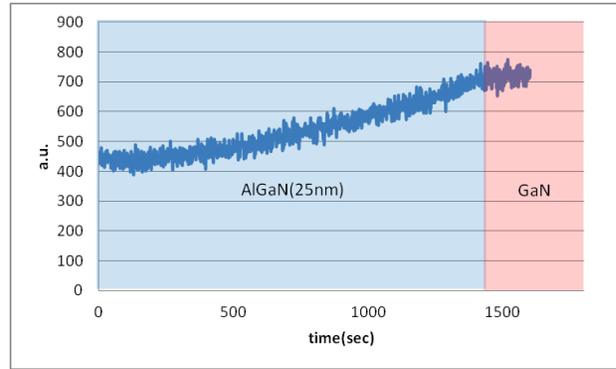


Figure 7. Intensity of reflected 364 nm light vs. time

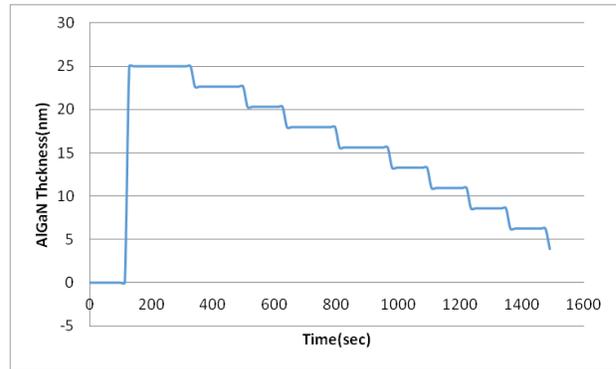


Figure 8. AlGaN thickness as a function of time (based on calculation)

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#### ACRONYMS

- MOS-FET: Metal Oxide Semiconductor-Field Effect Transistor
- HFET: Hetero-structure Field Effect Transistor
- GIT: Gate Injection Transistor
- 2DEG: 2-Dimensional Electron Gas
- ICP-RIE: Inductively Couple Plasma Reactive Ion Etching
- PECVD: Plasma Enhanced Chemical Vapor Deposition
- AFM: Atomic Force Microscopy